

Printed: Wednesday, August 24, 2005 7:25:36 PM

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Subject: clock distribution 100ps jitter requirement

The ultimate requirement on the timing jitter is the timing resolution that we are able to achieve in measurements with the whole electronics system. The current system design foresees one source for the clock to all of the HPTDCs in the system. One of the 4 THUBs will provide this "master" clock and distribute it to 3 "slave" THUBs. The baseline design for this assumes distribution over differential PECL lines and high quality RG58 pairs. A consideration mentioned during the review was to use twisted pair shielded cable for this.

The clocks are then distributed by each THUB to 31 TCPUs. Each TCPU is at the end of the TOF tray and distributes the clock to the TDIG cards on that tray over ribbon cables. On each stage of the distribution scheme the clock is regenerated via a high quality PLL.

A lot of this distribution scheme is already in place in the current system that was used in Run 5. The only board missing in our current system is the THUB board. The current TCPUs have almost all of the functionality that the future THUB will provide. So this scheme with the TCPU playing the role of the master clock can serve as a measure of how good this distribution scheme will work. We currently have 3 TCPUs in our setup, where one TCPU serves as the clock master and distributes its clock to the other two TCPUs over differential lines implemented via pairs of RG58 cables. The tray TCPU then distributes its clock to 8 TDIG boards with ribbon cables as in the essential model. The other two TPCUS have only one TDIG to which they distribute their clocks. With this system, we have achieved the 90ps timing resolution mentioned during the review.

The HPTDC chip receives a 40MHz input clock, which it regenerates internally (on the chip) with a PLL. The datasheet of the HPTDC specifies this input clock to have a jitter better than 100ps.

We have never measured the actual timing jitter we achieve at the input to the HPTDC. However, on the bench we have achieved a timing resolution on a cable delay measurement with both the start and stop measured on the same TDIG board of better than 20ps. An additional measurement that needs to be performed of course is to have the start and stop go to 2 different TDIG boards, where each TDIG board is served by a distributed clock as described above. A timing resolution measurement with this kind of setup of around 20ps would verify definitively that this distribution scheme works as expected, without actually measuring the jitter at the HPTDC input. Of course, we will look for means of qualifying this jitter. We can, however, estimate what the jitter should be at the input to the HPTDC from the specifications of the chips used in the current distribution scheme. I have tried to look up the datasheets of the relevant chips in this chain on the Web last night:

The ultimate clock source is the oscillator on the master TCPU. This

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chip is a CB3LV-3C at 40MHz. The timing jitter of this chip is given in the data sheet to be smaller than 1ps.

From there, the clock traverses several buffer and multiplexer chips which are in the Motorola family (like MC100EP56, MC100LVELT22). These chips are specified in their datasheets with 0.2ps jitter. On the slave TCPU, the clock is received by a MC100EP16 chip in PECL. This chip is specified to contribute 0.2ps jitter to the clock. It is then regenerated in a PLL from Silicon Labs, the Si5310 chip. The timing jitter at 40MHz for this chip is given as typically 3.7ps, with a maximum jitter of up to 15ps. From there, the clock is distributed to the TDIG boards in differential PECL format.

We don't know how much the cable run of about 7feet length (the longest run on the tray) contributes to the timing jitter, but I believe we can savely assume that the clock on TDIG will not have a jitter worse than 20 - 25ps. Finally, this clock is regenerated on the HPTDC chip with an on-chip PLL, which should again achieve a timing jitter better than 15ps, since the input clock is much better than the specification in the datasheet.

The longest cable run in this distribution scheme is about 100 feet and therefore a little longer than the final system will have, and consists of the RG58 cables that go from the Master TCPU on the tray (which is on the East side of the detector) to the start detector on the West side of the detector. We have not seen the phase of the East and the West start detector drift apart from the data we have taken during Run 5.

So the conclusion we have drawn from this is that our clock distribution scheme should provide a jitter performance that will meet the spec of the HPTDC chip.

Regards,
Jo Schambach